CLAIMS

What is claimed is:

1. A method of determining a DC margin of a latch, comprising:

performing a first simulation using a first simulation circuit to determine a trip voltage of a forward inverter of said latch;

performing a second simulation using a second simulation circuit to determine a one margin of said latch, said second simulation circuit comprising a worst case pull-up signal path; and

performing a third simulation using a third simulation circuit to determine a zero margin of said latch, said third simulation circuit comprising a worst case pull-down signal path .

2. The method of determining a DC margin of a latch in accordance with claim 1, further comprising:

determining said worst case pull-up signal path analytically by comparing a cumulative weighted resistance of at least one pull-up signal path to said latch.

3. The method of determining a DC margin of a latch in accordance with claim 2, wherein said step of determining said worst case pull-up signal path comprises:

identifying one or more pass circuit elements along each of possible pull-up signal paths;

determining a resistance of each of said identified one or more pass circuit elements based on respective sizes of said identified one or more pass circuit elements;

applying to said resistance, of each of said identified one or more pass circuit elements, a weight based on topology configuration of a corresponding one of said identified one or more pass circuit elements to produce one or more weighted resistance;

summing said one or more weighted resistance to produce said cumulative weighted resistance of each of said possible pull-up signal paths; and

determining said worst case pull-up signal path having a highest cumulative weighted resistance among said possible pull-up signal paths.

1   4. The method of determining a DC margin of a latch in accordance with claim 1, further

2 comprising:

3   determining said worst case pull-down signal path analytically by comparing a cumulative

4 weighted resistance of at least one pull-down signal path to said latch.

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6   5. The method of determining a DC margin of a latch in accordance with claim 4, wherein

7 said step of determining said worst case pull-down signal path comprises:

8   identifying one or more pass circuit elements along each of possible pull-down signal paths;

9   determining a resistance of each of said identified one or more pass circuit elements based

10 on respective sizes of said identified one or more pass circuit elements;

11   applying to said resistance, of each of said identified one or more pass circuit elements, a

12 weight based on topology configuration of a corresponding one of said identified one or more pass

13 circuit elements to produce one or more weighted resistance;

14   summing said one or more weighted resistance to produce said cumulative weighted

15 resistance of each of said possible pull-down signal paths; and

16   determining said worst case pull-down signal path having a highest cumulative weighted

17 resistance among said possible pull-down signal paths.

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19   6. The method of determining a DC margin of a latch in accordance with claim 1, wherein

20 said step of performing said second simulation comprises:

21   setting an initial value of an output, of a portion of said second simulation circuit representing

22 said latch, to a logical high;

23   applying a logical high pull-up input signal to an input, of said portion of said second

24 simulation circuit representing said latch, through said worst case pull-up signal path; and

25   determining a voltage level at said input.

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1   7. The method of determining a DC margin of a latch in accordance with claim 1, wherein

2   said step of performing said third simulation comprises:

3   setting an initial value of an output, of a portion of said third simulation circuit representing

4   said latch, to a logical low;

5   applying a logical low pull-down input signal to an input, of said portion of said third

6   simulation circuit representing said latch, through said worst case pull-down signal path; and

7   determining a voltage level at said input.

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9   8. A computer readable storage medium having stored thereon computer program for

10   implementing a method of determining a DC margin of a latch, said computer program comprising a

11   set of instructions for:

12   performing a first simulation using a first simulation circuit to determine a trip voltage of a

13   forward inverter of said latch;

14   performing a second simulation using a second simulation circuit to determine a one margin

15   of said latch, said second simulation circuit comprising a worst case pull-up signal path; and

16   performing a third simulation using a third simulation circuit to determine a zero margin of

17   said latch, said third simulation circuit comprising a worst case pull-down signal path .

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19   9. The computer readable storage medium according to claim 8, wherein said computer

20   program further comprising one or more instructions for:

21   determining said worst case pull-up signal path analytically by comparing a cumulative

22   weighted resistance of at least one pull-up signal path to said latch.

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1   10. The computer readable storage medium according to claim 9, wherein said computer

2   program further comprising one or more instructions for:

3   identifying one or more pass circuit elements along each of possible pull-up signal paths;

4   determining a resistance of each of said identified one or more pass circuit elements based

5   on respective sizes of said identified one or more pass circuit elements;

6   applying to said resistance, of each of said identified one or more pass circuit elements, a

7   weight based on topology configuration of a corresponding one of said identified one or more pass

8   circuit elements to produce one or more weighted resistance;

9   summing said one or more weighted resistance to produce said cumulative weighted

10 resistance of each of said possible pull-up signal paths; and

11   determining said worst case pull-up signal path having a highest cumulative weighted

12 resistance among said possible pull-up signal paths.

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14   11. The computer readable storage medium according to claim 8, wherein said computer

15 program further comprising one or more instructions for:

16   determining said worst case pull-down signal path analytically by comparing a cumulative

17 weighted resistance of at least one pull-down signal path to said latch.

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19   12. The computer readable storage medium according to claim 11, wherein said computer

20 program further comprising one or more instructions for:

21   identifying one or more pass circuit elements along each of possible pull-down signal paths;

22   determining a resistance of each of said identified one or more pass circuit elements based

23 on respective sizes of said identified one or more pass circuit elements;

24   applying to said resistance, of each of said identified one or more pass circuit elements, a

25 weight based on topology configuration of a corresponding one of said identified one or more pass

26 circuit elements to produce one or more weighted resistance;

27   summing said one or more weighted resistance to produce said cumulative weighted

28 resistance of each of said possible pull-down signal paths; and

29   determining said worst case pull-down signal path having a highest cumulative weighted

30 resistance among said possible pull-down signal paths.

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1   13. The computer readable storage medium according to claim 8, wherein said one or more

2   instructions for performing said second simulation comprises one or more instructions for:

3   setting an initial value of an output, of a portion of said second simulation circuit representing

4   said latch, to a logical high;

5   applying a logical high pull-up input signal to an input, of said portion of said second

6   simulation circuit representing said latch, through said worst case pull-up signal path; and

7   determining a voltage level at said input.

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9   14. The computer readable storage medium according to claim 8, wherein said one or more

10   instructions for performing said third simulation comprises one or more instructions for:

11   setting an initial value of an output, of a portion of said second simulation circuit representing

12   said latch, to a logical low;

13   applying a logical low pull-down input signal to an input, of said portion of said second

14   simulation circuit representing said latch, through said worst case pull-down signal path; and

15   determining a voltage level at said input.

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17   15. A simulation circuit for determining a DC margin of a latch, comprising:

18   a latch portion representing said latch being simulated, said latch portion comprising a

19   forward inverter and a feedback inverter, an input of said forward inverter being operably connected

20   to an input of said latch portion, and an input of said feedback inverter being operably connected to

21   an output of said latch portion;

22   a driver portion representing a driver circuit element capable of supplying an input signal to

23   said latch being simulated; and

24   a pass path subcircuit configured to receive a drive signal from said driver portion, and

25   configured to supply said drive signal to said input of said latch portion, said pass path subcircuit

26   representing one or more pass circuit elements along a worst case signal path between said driver

27   circuit element and said latch being simulated.

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29   16. The simulation circuit according to claim 15, wherein each of said forward inverter and

30   said feedback inverter comprises:

31   a complementary pair of field effect transistors.

1   17. The simulation circuit according to claim 15, wherein said pass path subcircuit

2 comprises:

3   one or more field effect transistors.

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5   18. The simulation circuit according to claim 17, wherein:

6   at least two of said one or more field effect transistors are arranged as a complementary

7 pair.

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9   19. The simulation circuit according to claim 17, wherein:

10   each of said one or more field effect transistors representing corresponding one of said one

11 or more pass circuit elements along a worst case signal path between said driver circuit element and

12 said latch being simulated; and

13   wherein sizes of said one or more field effect transistors are chosen based on respective

14 resistance of corresponding ones of said one or more pass circuit element.

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16   20. The simulation circuit according to claim 19, wherein:

17   each of said resistance is weighted based on a topology configuration of corresponding one

18 of said one or more pass circuit elements.

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